



## University Information & Software Selection Form

University Program 2006-1H

### Instructions

Please fill out this form completely and mark the software bundle selections you want, including additional binaries. **FAX this completed form pages 1 through 8**, along with the signed Policies document and a Purchase Order to: **Cheryl Mendenhall at (512) 342-5021**. You must also have an authorized university representative sign the License Agreement.

### Cadence Contact Information:

**Cheryl Mendenhall**

University Program Coordinator

Cadence Design Systems, Inc.

4516 Seton Center Parkway, Suite 300

Austin, TX 78759

Website: [http://www.cadence.com/support/university/ww\\_usp.aspx](http://www.cadence.com/support/university/ww_usp.aspx)

Phone: (512) 342-5350

Fax: (512) 342-5021

Email: [cherylm@cadence.com](mailto:cherylm@cadence.com)

### University Information

Date: \_\_\_\_\_

University: \_\_\_\_\_

Licensing Professor: \_\_\_\_\_

Dept: \_\_\_\_\_

Address: \_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

Phone: \_\_\_\_\_ Fax: \_\_\_\_\_

Email: \_\_\_\_\_

### Technical Liaisons

Primary: \_\_\_\_\_ Secondary: \_\_\_\_\_

Dept: \_\_\_\_\_ Dept: \_\_\_\_\_

Address: \_\_\_\_\_ Address: \_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

Phone: \_\_\_\_\_ Phone: \_\_\_\_\_

Fax: \_\_\_\_\_ Fax: \_\_\_\_\_

Email: \_\_\_\_\_ Email: \_\_\_\_\_

**A web site pertaining to your use of Cadence software is required!**

URL: \_\_\_\_\_

### Server Platform Configuration Information

SUN (Solaris)  HP (HP-UX)  IBM (AIX)  RedHat (Linux)  Windows

Model: \_\_\_\_\_ OS Version: \_\_\_\_\_

HOST ID: \_\_\_\_\_



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### Custom Integrated Circuits Bundle

Estimated number of licenses needed: \_\_\_\_\_

**Executables for:**     SUN (Solaris)    HP (HP-UX)    IBM (AIX)    RedHat (Linux)

<u>Class or Research?</u>	<u>Title of Class or Research Project</u>	<u>Students with Cadence Access</u>
_____	_____	_____
_____	_____	_____
_____	_____	_____

### The Custom IC Bundle Software Reference List:

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
<b>Design Environment</b>		
Virtuoso <sup>R</sup> analog design environment	34510	IC 5.1
Virtuoso <sup>R</sup> AMS designer environment	70000	IC 5.1
Virtuoso <sup>R</sup> specification driven environment (VSDE) <sup>1</sup>	35100	VSDE 4.1
Virtuoso <sup>R</sup> characterization & modeling option for VSDE <sup>1</sup>	35200	VSDE 4.1
Virtuoso <sup>R</sup> NeoCircuit DFM <sup>1</sup>	3806	Neockt 3.3
<b>Design Entry</b>		
Cadence <sup>R</sup> SKILL development environment	900	IC 5.1
Virtuoso <sup>R</sup> schematic VHDL interface	21060	IC 5.1
Virtuoso <sup>R</sup> schematic editor Verilog <sup>R</sup> interface	21400	IC 5.1
Virtuoso <sup>R</sup> schematic editor	34500	IC 5.1
Virtuoso <sup>R</sup> analog Oasis run-time option	32100	IC 5.1
<b>Layout</b>		
Virtuoso <sup>R</sup> Compactor	305	IC 5.1
Virtuoso <sup>R</sup> -XL layout editor <sup>2</sup>	3000	IC 5.1
Virtuoso <sup>R</sup> customer placer	-- included in product 3000 --	
Cadence <sup>R</sup> chip assembly router <sup>3</sup>	3300	ICC 11.2
Virtuoso <sup>R</sup> NeoCell analog physical synthesis <sup>4</sup>	3905	Neocell 3.4

<sup>1</sup> not available on IBM

<sup>2</sup> includes CIF reader/writer and Virtuoso Stream Interface

<sup>3</sup> includes GDSII/EDIF and LEF/DEF interfaces

<sup>4</sup> not available on IBM



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### The Custom IC Bundle Software Reference List, continued

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
<b>Physical Verification</b>		
Dracula <sup>R</sup> graphical user interface	365	IC 5.1
Cadence <sup>R</sup> RC network reducer option	681	IC 5.1
Dracula <sup>R</sup> physical verification and extractor suite	70520	IC 5.1
Diva <sup>R</sup> physical verification and extractor suite	71520	IC 5.1
Assura <sup>TM</sup> design rule checker	72110	Assura 3.1.5
Assura <sup>TM</sup> layout vs. schematic verifier	72120	Assura 3.1.5
Assura <sup>TM</sup> parasitic extractor	72130	Assura 3.1.5
Assura <sup>TM</sup> RCX field solver option	72131	Assura 3.1.5
Assura <sup>TM</sup> RCX parasitic inductance option	72132	Assura 3.1.5
Assura <sup>TM</sup> RCX Multiprocessor option	72133	Assura 3.1.5
Assura <sup>TM</sup> RCX High Frequency Option	72134	Assura 3.1.5
Assura <sup>TM</sup> RF Bundle	72135	Assura 3.1.5
Assura <sup>TM</sup> RCX Parasitic Inductance: Cell Level Option	72136	Assura 3.1.5
Assura <sup>TM</sup> Graphical User Interface Option	72140	Assura 3.1.5
Assura <sup>TM</sup> multiprocessor option	72150	Assura 3.1.5
RCX Advanced process features	72138	AV 3.1.4NM
Pcell Generator <sup>2</sup>	PASPCG	PAS 3.1
Graphical Technology Editor <sup>2</sup>	PASGTE	PAS 3.1
Generator for Assura <sup>TM</sup> compatible verification decks <sup>2</sup>	PASASG	PAS 3.1
Generator for Diva <sup>R</sup> compatible verification decks <sup>2</sup>	PASDIG	PAS 3.1
Generator for Dracula <sup>R</sup> compatible verification decks <sup>2</sup>	PASDRG	PAS 3.1
Error Cell Generator <sup>2</sup>	PASECG	PAS 3.1

<sup>2</sup> not available on IBM or HP

Releases Assura 3.1.5, IC 5.1, ICC 11.2, IUS 5.6, MMSIM 6.0, Neocell 3.4, Neockt 3.3, PAS 3.1, VSDE 4.1

### The Custom IC Bundle Software Reference List, continued



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<b><u>Product</u></b>	<b><u>Product No.</u></b>	<b><u>Release Stream</u></b>
<b>Circuit Simulation</b>		
Virtuoso <sup>R</sup> schematic editor HSPICE interface <sup>1</sup>	276	IC 5.1
Virtuoso <sup>R</sup> schematic editor Spectre <sup>R</sup> interface	-- included in product 32500 --	
Virtuoso <sup>R</sup> electronic design for manufacturability option	32120	IC 5.1
Cadence <sup>R</sup> SPICE	32150	IC 5.1
Virtuoso <sup>R</sup> Spectre <sup>R</sup> analog circuit simulator	32500	MMSIM 6.0
Virtuoso <sup>R</sup> UltraSim full chip simulator	33500	MMSIM 6.0
Virtuoso <sup>R</sup> Spectre <sup>R</sup> RF simulation option	32520	MMSIM 6.0
Virtuoso <sup>R</sup> analog HSPICE interface option <sup>1</sup>	32760	IC 5.1
Virtuoso <sup>R</sup> AMS designer simulator	70001	IUS 5.6
<b>Interfaces</b>		
Virtuoso <sup>R</sup> schematic composer to design compiler integration	570	IC 5.1
Virtuoso <sup>R</sup> EDIF 200 reader	940	IC 5.1
Virtuoso <sup>R</sup> EDIF 200 writer	945	IC 5.1
Virtuoso <sup>R</sup> EDIF 300 connectivity reader/writer	952	IC 5.1
Virtuoso <sup>R</sup> EDIF 300 schematic reader/writer	953	IC 5.1
Cadence <sup>R</sup> design framework integrator's toolkit	12141	IC 5.1

<sup>1</sup> requires additional licenses that must be obtained from Synopsys

Releases Assura 3.1.5, IC 5.1, ICC 11.2, IUS 5.6, MMSIM 6.0, Neocell 3.4, Neockt 3.3, PAS 3.1, VSDE 4.1



## University Information & Software Selection Form

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### Digital Integrated Circuits Bundle

Estimated number of licenses needed: \_\_\_\_\_

**Executables for:**     SUN (Solaris)     HP (HP-UX)     IBM (AIX)     RedHat (Linux)

<u>Class or Research?</u>	<u>Title of Class or Research Project</u>	<u>Students with Cadence Access</u>
_____	_____	_____
_____	_____	_____
_____	_____	_____

### The Digital IC Bundle Software Reference List

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
<b>Place &amp; Route and Timing</b>		
Virtuoso <sup>R</sup> -XL layout editor	3000	IC 5.1
Cadence <sup>R</sup> chip assembly router	3300	ICC 11.2.41
Silicon Ensemble <sup>TM</sup> PKS optimization <sup>1,2</sup>	SPR002	SOC 5.2
<b>Physical Verification</b>		
Dracula <sup>R</sup> physical verification and extractor suite	70520	IC 5.1
<b>Design for Manufacturing</b>		
Fire & Ice QXC (gate)	QXC1	EXT5.1
VoltageStorm (gate and transistor)	VS2	SEV4.1
<b>Signal Integrity</b>		
CeltIC NDC crosstalk analyzer with delay calculator	CM00500	TSI 4.2
PacifiC static noise analyzer for custom digital ICs	CM00100	TSI 4.2
SignalStorm NDC nanometer delay calculator	SGSNDC	TSI 5.2
SignalStorm library characterizer	SLC1	TSI 5.2
<b>Silicon Virtual Prototyping</b>		
Cadence <sup>R</sup> SOC Encounter Global Physical Synthesis (GPS)	FE200GPS	SOC 5.2
Route accelerator multi-threaded route option	RA100	SOC 5.2
<b>Test</b>		
Encounter <sup>R</sup> test architect XL	ET001	ET 3.1
Encounter <sup>R</sup> true time test GXL	ET002	ET 3.1
Encounter <sup>R</sup> diagnostics GXL	ET004	ET 3.1

<sup>1</sup> not available on Linux

<sup>2</sup> includes CT-Gen

Releases ANLS 5.2, ET 3.1, IC 5.1, ICC 11.2.41, SOC 5.2, TSI 4.2, TSI 5.2



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### Verification Bundle

Estimated number of licenses needed: \_\_\_\_\_

**Executables for:**     SUN (Solaris)    HP (HP-UX)    IBM (AIX)    RedHat (Linux)

<u>Class or Research?</u>	<u>Title of Class or Research Project</u>	<u>Students with Cadence Access</u>
_____	_____	_____
_____	_____	_____
_____	_____	_____

### The Verification Bundle Software Reference List

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
<b>Functional Verification</b>		
Cadence <sup>R</sup> NC-Verilog <sup>R</sup> simulator	28200	IUS 5.6
Cadence <sup>R</sup> NC-VHDL simulator	28400	IUS 5.6
Cadence <sup>R</sup> NC-Sim mixed language simulator <sup>1</sup>	28000	IUS 5.6
Cadence <sup>R</sup> simulation analysis environment	25010	IUS 5.6
Incisive <sup>TM</sup> unified simulator <sup>2</sup>	29300	IUS 5.6
AMS option to Incisive <sup>2</sup>	29370	IUS 5.6
FormalCheck <sup>R</sup> model checker <sup>3</sup>	V29	IUS 5.3
<b>Verification Process Automation</b>		
SpecMan Elite	SPCMN1000	SPMN 5.0
SureCov	SCOV1000	SCOV 4.0
Incisive <sup>TM</sup> enterprise manager <sup>1,2</sup>	VMGR1000	VMGR 1.3
Incisive <sup>TM</sup> enterprise eAnalyzer	ENLZR1000	EANL 5.0.2
<b>Formal Verification</b>		
Encounter <sup>TM</sup> Conformal GXL	CFM300	CONFRML 5.2
<b>Synthesis</b>		
Encounter <sup>TM</sup> RTL Compiler Ultra <sup>4</sup>	RC200	RC 5.2

<sup>1</sup> not available on IBM<sup>2</sup> not available on Windows 2000<sup>3</sup> not available on IBM, Windows 2000 or Linux<sup>4</sup> not available on HP or Windows 2000

Releases CONFRML 5.2, EANL 5.0.2, EVCAMBA 2.2, EVCAXI 1.2, EVCETH 2.2, EVCPCI 2.11, EVCPCIE 2.1, EVCPCIR 2.0, EVCPCIX 2.1, EVCUSB 2.2, IUS 5.3, IUS 5.6, RC 5.2, SCOV 4.0, SPMN 5.0, VMGR 1.3



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### The Verification Bundle Software Reference List, continued

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
<b>Pre-verified, Re-usable Verification IP Components</b>		
AMBA AHB protocol	EVC1000	EVCAMBA 2.2
USB protocol	EVC1001	EVCUSB 2.2
PCI Express End Point protocol	EVC1002	EVCPCIE 2.1
PCI Express Root Complex protocol	EVC1003	EVCPCIE 2.1
PCI 2.2/2.3 protocol	EVC1004	EVCPCI 2.11
PCI-X 1.0/2.0 protocol	EVC1005	EVCPCIX 2.1
Ethernet protocol	EVC1006	EVCETH 2.2
AMBA AXI protocol	EVC1007	EVCAXI 1.2

Releases CONFRML 5.2,EANL 5.0.2, EVCAMBA 2.2, EVCAXI 1.2, EVCETH 2.2 EVCPCI 2.11  
EVCPCIE 2.1 EVCPCIR 2.0, EVCPCIX 2.1, EVCUSB 2.2, IUS 5.3, IUS 5.6, RC 5.2, SCOV 4.0, SPMN 5.0, VMGR 1.3



## University Information & Software Selection Form

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### Silicon-Package-Board Bundle

Estimated number of licenses needed: \_\_\_\_\_

**Executables for:**     SUN (Solaris)    HP (HP-UX)    IBM (AIX)    RedHat (Linux)    Windows

<u>Class or Research?</u>	<u>Title of Class or Research Project</u>	<u>Students with Cadence Access</u>
_____	_____	_____
_____	_____	_____
_____	_____	_____

### The Packaging & Board Bundle Software Reference List

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
<b>PCB Design and Layout</b>		
Allegro <sup>R</sup> PCB librarian 610	PX3500	SPB 15.5.1
Allegro <sup>R</sup> PCB design HDL 610	PX3700	SPB 15.5.1
Allegro <sup>R</sup> PCB design CIS 610 <sup>1</sup>	PX3710	SPB 15.5.1
<b>PCB High-Speed Analysis</b>		
Allegro <sup>R</sup> PCB SI 610	PX3100	SPB 15.5.1
<b>IC Packaging</b>		
Allegro <sup>R</sup> Package Designer 620	PA6620	SPB 15.5.1
Allegro <sup>R</sup> Package SI 620	PA7620	SPB 15.5.1
<b>Orcad Family</b>		
Allegro <sup>R</sup> PCB design HDL 220	PS3000	SPB 15.5.1
Allegro <sup>R</sup> PCB design CIS 220 <sup>1</sup>	PS3010	SPB 15.5.1
Allegro <sup>R</sup> AMS simulator 210 <sup>1,3</sup>	PS2200	SPB 15.5.1
Layout Studio <sup>1</sup>	PS1430	SPB 15.5.1

<sup>1</sup> available only on Windows 2000 (can be served from a Unix license server)

<sup>2</sup> not available on IBM or Linux

<sup>3</sup> superset of Pspice and Advanced Analysis Option

Release SPB 15.5.1